



Security Lithography

Source: <https://semiengineering.com/manufacturing-bits-march-3-2/>
MARCH 3RD, 2020 - BY: [MARK LAPEDUS](#)

At the recent SPIE Advanced Lithography conference, Multibeam disclosed more details about its efforts to develop multi-beam direct-write lithography [for chip security applications](#).

David Lam, chief executive and chairman of Multibeam, described how multi-beam lithography can be used to help thwart IC counterfeiting and tampering in the market. This lithography technology can be used to embed a unique ID into each IC during wafer fabrication.

Needless to say, security is a major concern in the semiconductor industry. “We know there are some very determined hackers out there. They can use very sophisticated tools to delayer your chip one layer at a time until they see it,” Lam said. “Counterfeit ICs remain a major problem throughout the semiconductor supply chain. Each critical IC should have a unique tamper-proof identifier to enable verification of authenticity throughout its life cycle, but current anti-counterfeit solutions are costly and fall far short of expectations.”

Nonetheless, Multibeam’s lithography technology is different than optical and extreme ultraviolet (EUV) lithography systems. Both optical and EUV require a photomask to pattern a chip. A photomask is a separate component, which is basically a master template for an IC design. At advanced nodes, the photomask is complex and expensive.

For years, the industry has been developing and selling various lithography systems, which do not require an expensive photomask. This includes what’s commonly called direct-write or maskless lithography.

Originally developed by IBM in the 1980s, direct-write lithography makes use of a single-beam e-beam tool that directly patterns tiny features on a wafer. But the throughputs for e-beam lithography are slow, making it too expensive for volume production. So single-beam direct-write tools are relegated to niche applications.

To solve the throughput problem, the industry has been developing direct-write e-beam systems using multiple beams. Several companies have tried to develop this technology. Most have failed due to technical issues.

Multibeam is still pursuing it. Unlike conventional direct-write lithography systems, which employ a single complex e-beam column, Multibeam takes a multi-column approach. Assembled in an array, Multibeam’s multi-column technology is capable of writing patterns directly on the wafer.

At SPIE, Multibeam described a four-module system. It can be upgraded to six modules. “Basically, we can do 60 wafers per hour with a six-module system,” Lam said.

With the technology, Multibeam is focusing on two areas—full-wafer maskless lithography and security. Full-wafer maskless lithography involves patterning a wafer using Multibeam’s tools. For this, the company is focusing its efforts on more mature nodes, namely 45nm and 28nm. “If you look at the spectrum, our sweet spot is 45nm and above from a node standpoint,” Lam said. Multibeam plans to address advanced nodes down the road.

“The second sweet spot is security,” Lam said. “We will start off with the secure chip ID market. Later on, we will expand into what we call on-chip security.”

In security, though, there are already well-entrenched solutions in the IC market. For some time, the IC industry has used traditional non-volatile memory for secure code storage applications. This memory can store a few bits of authentication information for security purposes using electric-fuse (eFuse) or anti-fuse technology.

The current solutions may not always be full-proof. “The other challenge is that it needs custom fab processing. Then, you have three or four masks to do that. So, you need extra mask steps. And then you also need the drive circuit to activate, implement and provision it. And then finally, people wonder if you can shrink it,” Lam said.

That’s where Multibeam’s technology fits in. Lam calls this “security lithography.” Basically, using multi-beam technology, Multibeam’s system can pattern and embed a unique ID inside each IC during fabrication. The system hard codes the ID at the silicon level, making it tamper-proof. The information can link to a secure database to store individual chip data.

“We recommend doing this at the lowest layer of vias. But you can do it at other layers too. Our system doesn’t require special experience or custom processing. There is no impact on die size or functionality,” Lam said.

Contact

Ted Prescop

Sr. Director - Technology Applications

Phone: 408-980-1800 Ext.3

Email: tprescop@multibeamcorp.com
