E-Beam to Complement Optical Lithography for 1D Layouts

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ABSTRACT

The semiconductor industry is moving to highly regular designs, or 1D gridded layouts, to enable scaling to advanced nodes, as well as improve process latitude, chip size and chip energy consumption.

The fabrication of highly regular ICs is straightforward. Poly and metal layers are arranged into 1D layouts. These 1D layouts facilitate a two-step patterning approach: a line-creation step, followed by a line-cutting step, to form the desired IC pattern (See Figure 1).

The first step, line creation, can be accomplished with a variety of lithography techniques including 193nm immersion (193i) and Self-Aligned Double Patterning (SADP)[1]. It appears feasible to create unidirectional parallel lines to at least 11 nm half-pitch, with two applications of SADP for pitch division by four. Potentially, this step can also be accomplished with interference lithography or directed self assembly in the future.

The second step, line cutting, requires an extremely high-resolution lithography technique. At advanced nodes, the only options appear to be the costly quadruple patterning with 193i, or EUV or E-Beam Lithography (EBL).

This paper focuses on the requirements for a lithography system for "line cutting", using EBL to complement Optical. EBL is the most cost-effective option for line cutting at advanced nodes for HVM.

Keywords: Lithography, E-Beam, EBDW, ML2, NGL, CEBL, DFM, SADP, EBL

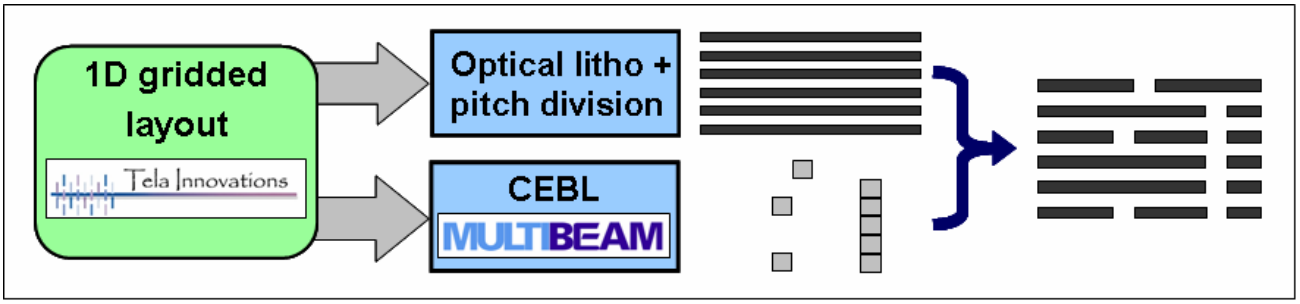

Figure 1: E-Beam and Optical lithography both have strengths and weaknesses. 1D layouts enable a complementary lithography approach that draws on the strengths of both Optical and E-beam lithography.

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1. INTRODUCTION

The semiconductor industry has had great success in shrinking chip geometries, enabling continuous scaling with Moore's law. To stay competitive, chip manufacturers are compelled to find new ways to shrink transistor cost year over year. Optical lithography has played a major role in this effort.

The most advanced optical lithography is 193nm ArF immersion technology, or 193i. Today, 193i is the only mature lithography technology capable of producing leading-edge chips in HVM. However, 193i is reaching limits in resolution, and the cost of extending 193i beyond the 20nm half-pitch is expected to increase dramatically.

2. LOGIC DFM TRENDING TO 1D GRIDDED LAYOUTS

To make Logic and SOC (System-on-Chip) devices manufacturable beyond 20nm half-pitch, designers are moving toward a new 1D layout style.

Intel migrated to 1D layouts when scaling from the 65nm node to the 45nm node, enabling the use of mature optical litho technology[2]. Last year, TSMC announced the conversion of 65nm node libraries to 1D layouts in collaboration with Tela Innovations[3]. IBM appears to be moving toward highly regular layouts with one-direction and a fixed-pitch for Logic manufacturability[4]. The new 1D layouts are used for critical layers, where optical resolution limits pose the greatest challenge. Critical layers include line-cuts, via holes and contact holes, which are all low-pattern density.

In 1D gridded layouts, each metal layer runs perpendicular to the poly or metal layer below it. Contacts or vias provide connections between layers (See Figure 2).

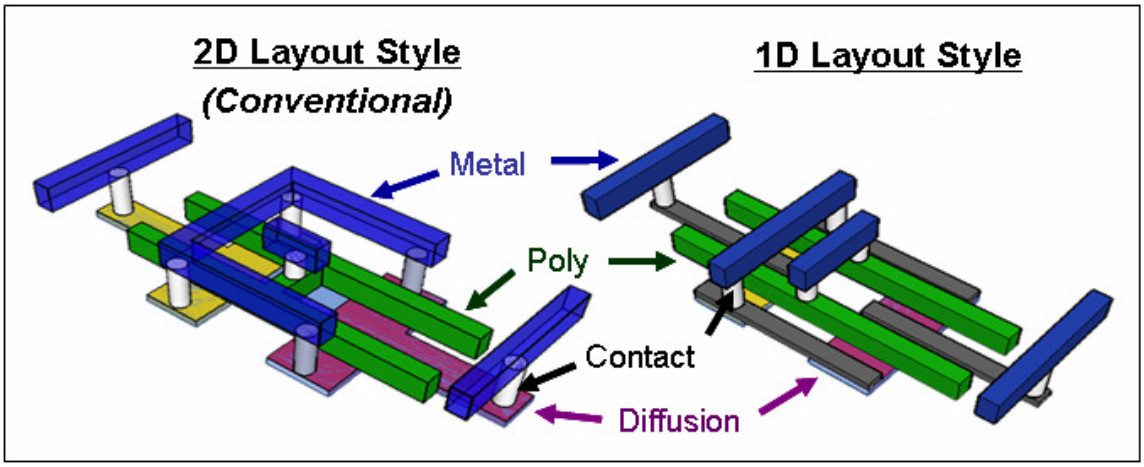

Figure 2: Conversion of CMOS layout from traditional 2D design to 1D layout.

The 1D layout for Logic and SOC devices eliminates serious problems encountered in subwavelength lithography including optical proximity and spatial frequency effects[5]. 1D layouts simplify design rules, and increase process window. Some of the other benefits of 1D layouts are shown in Table 1. A reduction in chip size is shown in Figure 3.

1D layouts are being implemented for an increasing number of critical layers. Sam Sivakumar of Intel noted, "Gridded layouts have now become ubiquitous -- the way of the future."[6]

Table 1. Benefits of 1D Gridded Layouts at 90nm technology node.

	2D Layout	1D Layout	1D Improvement
Average Cell Area (um^2)	14.25	12.66	15.5% smaller
Routed Block Area (mm^2)	0.12	0.095	20.5% smaller
Avg. Max. Operating Frequency (MHz)	147	262	78% faster
Yield (%)	57	68	19% higher yield

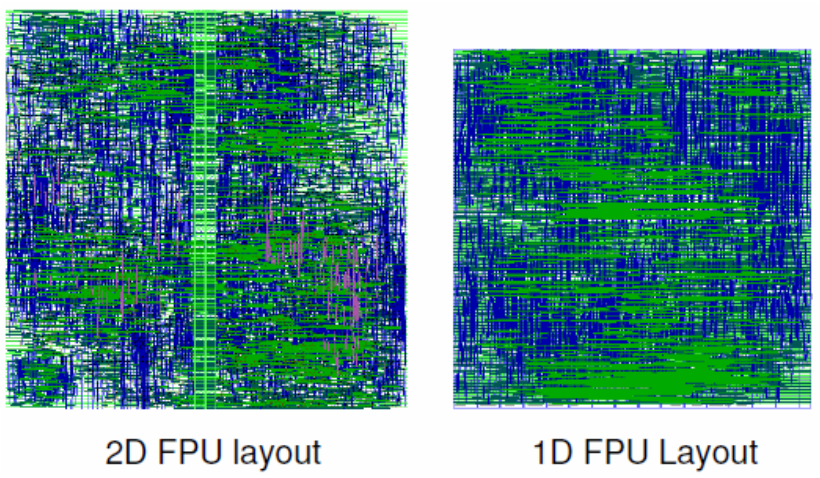

Figure 3: Comparison of chip size for 2D and 1D layouts of FPU (floating-point unit).

3. THE CONCEPT OF COMPLEMENTARY LITHOGRAPHY

The 1D layout style lends itself to a two-step approach. First, pattern a regular array of uniform high-density lines, with small line-width roughness. Then, cut the lines with a sparse but extremely high-resolution pattern. Since each of these steps is separate and discreet, we have the ability to choose the best lithography technology for each step.

The first step, creating the lines, is accomplished with a variety of lithography techniques including Optical lithography and Self-Aligned Double Patterning (SADP), or, in the future, interference lithography or directed self assembly. SADP has been demonstrated to work for 11nm half-pitch, with two applications of SADP for pitch division by four.

The second step, line cutting, will require a high-resolution lithography technique at advanced nodes, such as EUV or EBL (E-Beam Lithography). Having different lithography technologies working hand-in-hand is known as "Complementary Lithography", an approach introduced by Yan Borodovsky of Intel in 2010.

Optical lithography offers the most mature and cost-effective solution to pattern unidirectional, interference-like parallel lines; EBL offers the most cost-effective way to cut the lines at advanced technology nodes (e.g. 20nm half-pitch and beyond). Thus, Complementary Lithography takes advantage of the best of both optical litho and EBL to pattern next generation semiconductors.

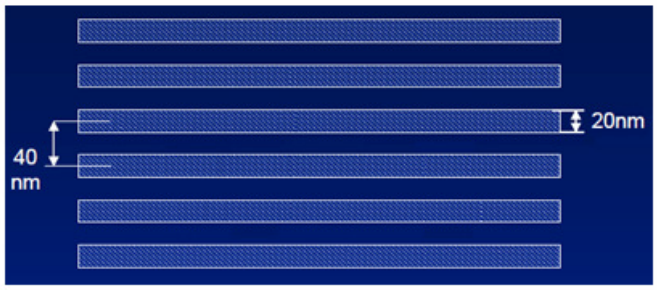

Figure 4: 20 nm line/space pattern with optical lithography and pitch doubling. [7]

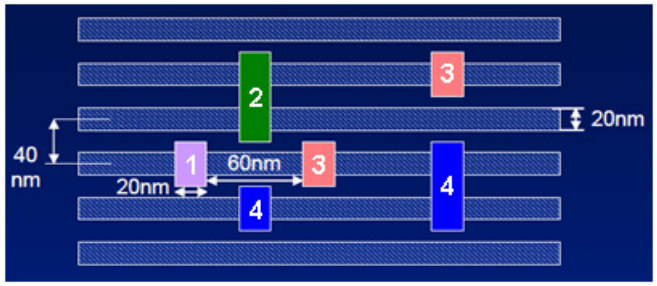

Figure 5: Intel approach for 20nm line/space. This can be accomplished with 4 optical cut masks, or 1 cut mask with EUV, or 0 masks with EBL.[7]

4. COMPLEMENTARY E-BEAM LITHOGRAPHY (CEBL)

CEBL (Complementary E-Beam Lithography) refers to EBL being used in Complementary Lithography. CEBL is not a brand name or trademark, but a term used in a way similar to CMOS (Complementary Metal Oxide Semiconductor).

In Complementary Lithography, CEBL is used to pattern critical layers (including line cuts, via holes and contact holes). Optical lithography is used for all other layers. Thus, CEBL extends the useful life of Optical Lithography, while drastically reducing the cost of manufacturing advanced Logic and SOC devices.

In CEBL, e-beam lithography technology provides the urgently needed solution to the industry's most challenging problems in lithography at 20nm half pitch and beyond. [8]

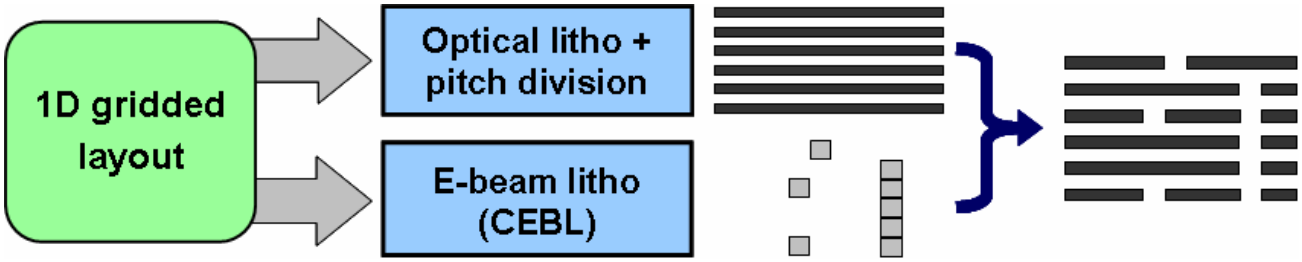

Figure 6: This shows Complementary E-Beam Lithography (CEBL) used hand-in-hand with Optical. A layout with 40nm pitch requires Optical litho with four "cut" masks, or E-Beam Lithography with zero "cut" masks.

5. IMPLEMENTATION OF CEBL

A dedicated CEBL lithography system must pattern with high resolution, high overlay accuracy and high throughput, at a reasonable cost.

5.1 High 2D resolution

Extremely high resolution has been demonstrated with e-beam lithography, including sub-10nm lithography in resist.[9] An e-beam lithography system can pattern line cuts with high overlay accuracy in a single pass, eliminating costly optical "cut" masks.

Feature resolution is largely limited by two factors: electron-electron repulsion within the e-beam column, and electron scattering in the resist.

5.1.1 Beam broadening due to electron-electron repulsion

Electron-electron repulsion (also known as Coulomb repulsion) within an e-beam column is exacerbated by high e-beam current (electron density) and low e-beam energy (electron travel time). Higher resolution can be achieved by reducing the beam current and increasing the beam energy.

However, if beam current is reduced too much, throughput suffers. To achieve 5 wph throughput for line-cutting, total average beam current of greater than 1 μA is required. Multibeam uses 15 to 30 nA per column in a multi-column system with 100 columns to achieve total beam current of 1.5 to 3 μA.

In a typical e-beam column at 5 keV beam energy and 20 nA beam current, beam broadening due to Coulomb repulsion can be much larger than 11 nm. To reduce this effect, beam energy should be above 5 keV. For example, at beam energy of 10 keV, beam broadening in a typical column is reduced to ~ 4 nm.

5.1.2 Beam broadening due to electron-resist interactions

Regardless of column design, electron interactions in resist result in pattern blur (also known as image blur), thus limiting the minimum feature size that can be patterned in e-beam lithography.

At low beam energy, minimum feature size is primarily determined by forward scattering of incoming electrons. According to a study by Cord, "the minimum achievable feature size will ultimately be limited by the point-spread function (PSF) of the exposing radiation, rather than the contrast of the development process."[10] Forward scattering (point spread) in resist is limited by increasing the e-beam energy and reducing the resist thickness. To achieve the highest possible resolution in low-energy e-beam lithography, it is necessary to use a very thin resist.

Unfortunately, it is not possible to make the resist arbitrarily thin. There are three factors to take into consideration: resist defect density (pinholes), resist thickness uniformity, and the need for a conductive coating to minimize charging. If the wafer has step height (topography) variations in the range of 25 nm, a resist thickness of 50 nm or greater may be required. This limits the minimum feature size printable with e-beam lithography at low beam energy (< 10 keV), independent of beam current, or beam spot size. For this reason, >10 keV beam energy is necessary for CEBL at advanced nodes.

5.2 Overlay accuracy

In this paper, we examine two major factors in overlay accuracy: e-beam drift and wafer thermal expansion.

5.2.1 Beam Drift

The e-beam can drift for a variety of reasons. In system design and operation, every attempt should be made to minimize drift (e.g. shielding from environmental effects, minimizing contamination and charging, stabilizing the temperature in the electronics and column, etc).

Realistically, there will always be some beam drift. Regardless of its cause, we mitigate beam drift with repeat alignments. In CEBL, the e-beam must remain well aligned within the 10 minute write time for each wafer.

E-beam litho and Optical litho are able to share similar methods for global (off-axis) alignment using optical techniques. In addition, Multibeam is implementing local (in situ) alignment. Every Multibeam column is capable of operating in "SEM mode". SEM mode enables direct in-process beam-to-wafer alignment, correcting for beam drift. This is possible because each column has only one beam.

5.2.2 Thermal stability

High-energy e-beam lithography may result in overlay errors due to wafer thermal expansion. In Figure 7, Multibeam estimated thermal expansion of a 300mm wafer at various beam energies. E-beam energy above 15 keV (e.g. 50 keV) leads to major challenges in heat removal, thermal stability and wafer expansion-induced overlay error. If beam energy is > 15 keV, wafer expansion will necessitate frequent re-registration during wafer patterning.

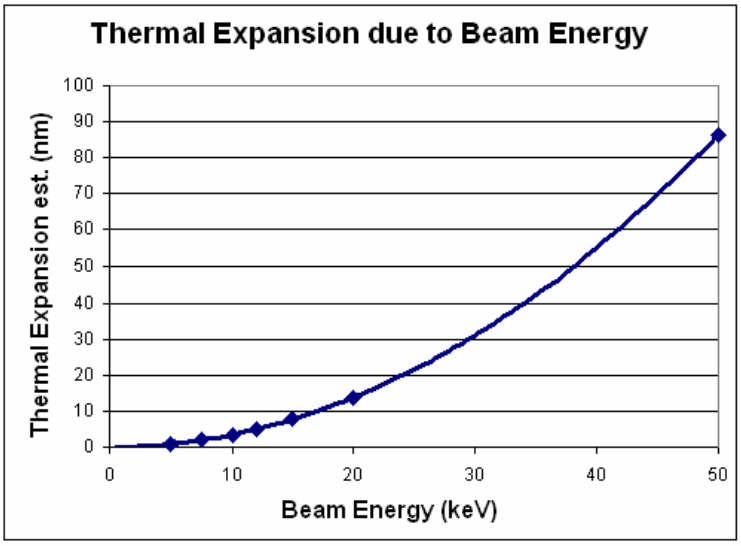

Figure 7. Thermal expansion of 300mm wafer due to e-beam energy.

5.3 Summary of optimal operating region for CEBL in HVM[11]

The optimal operating region for CEBL is bounded by resolution limitations due to Coulomb repulsion and electron-resist interactions, as well as overlay limitations due to wafer expansion. The optimal region may shift for a variety of reasons: it may shift left or right with column design modifications, shift down with resist improvements, or shift up with improved alignment and temperature control. However, there will always be a bounded optimal region for best resolution and overlay in CEBL.

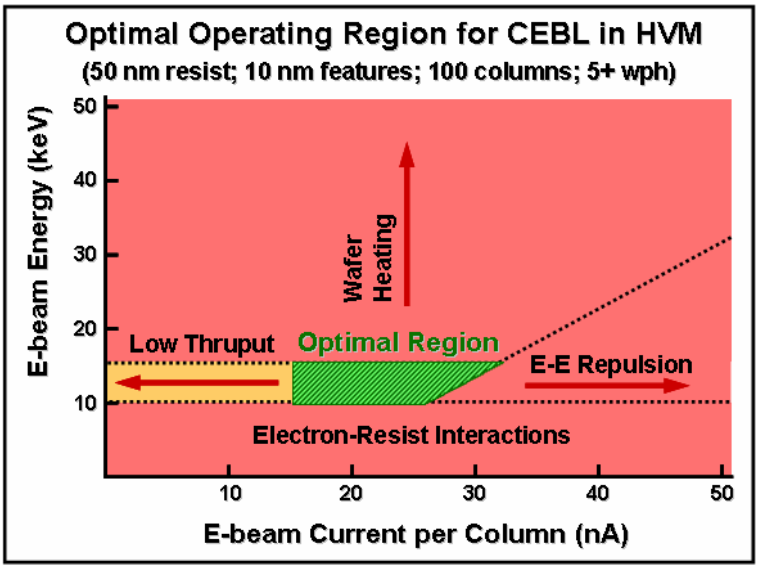

Figure 8. The optimal operating region for a typical column designed for CEBL ranges from 10 keV to 15 keV beam energy and 15 to 30 nA beam current per column.

5.4 High throughput

E-beam lithography's low throughput is well known. This is the main reason why e-beam litho isn't used in high volume manufacturing today. By focusing on CEBL instead of trying to pattern every layer, we boost throughput and reduce cost. However, even with CEBL, we must drastically increase throughput.

Multibeam starts with an innovative column design that is both small and fast. The column is optimized for CEBL with 10–15 keV beam energy. The column design is all-electrostatic (no magnets). The elimination of the magnetic coil makes the column footprint very small. In the absence of magnetic fields (and hysteresis), the e-beam is deflected at very high speeds for vector-scan beam positioning.

With ~100 columns (for 300mm wafers) in each module and 10 modules in a cluster tool, Multibeam immediately achieves 1000x gain in throughput. The cluster tool with 10 modules has the same footprint as an optical tool.

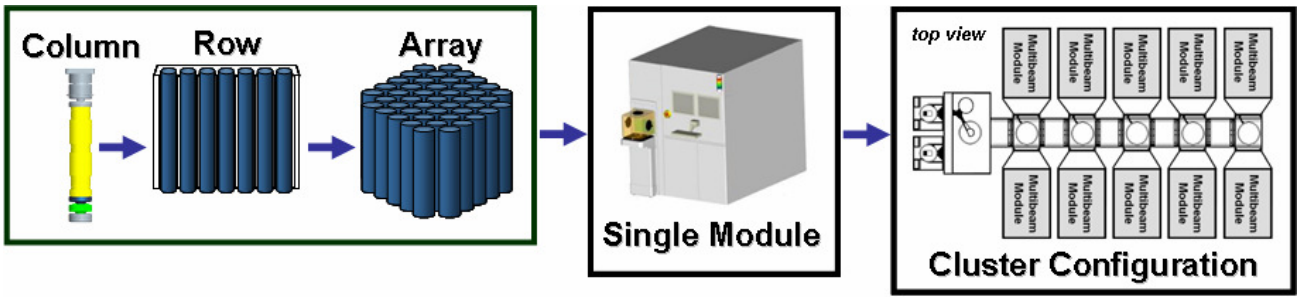

Figure 9. Multibeam scalable architecture. Multibeam optimizes a single column before building an Array of identical columns. A module with a single column array is capable of patterning 5 wafers per hour. A cluster tool is capable of patterning 50 wafers per hour.

Multibeam achieves higher throughput with vector-scanned shaped beams to pattern critical layers only (i.e. via and contact holes, as well as line-cuts).

Vector scanning offers a huge throughput advantage when patterning critical layers, which have low pattern density. With vector scanning, Multibeam skips over empty areas, reduces shot count and data rate, and maximizes beam "on" time. This results in a 10x improvement in throughput when compared to 40-50% pattern density.

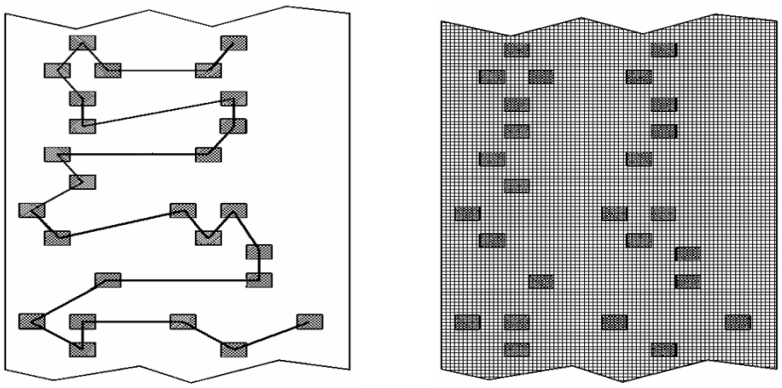

Figure 10: Comparison of Vector-scan and Raster-scan approaches. On left, the vector-scanned beam patterns an entire field with 45 high-speed flashes as it jumps over empty areas between flashes. On right, > 90% of beamlets are "off" while > 900 pixels are flashed for the same pattern.

Multibeam's approach achieves additional throughput gains with: a) High beam current with one electron source per beam; b) in-process e-beam position registration with in-situ SEM; c) Energy selection optimized at 10–15 keV; and d) co-optimization with chip designers, process engineers, and optical litho equipment.

5.5 Cost effectiveness

Multibeam's product development is significantly lower in cost compared to other approaches. Multibeam achieves this by focusing on a single application: CEBL for HVM. CEBL requires patterning only a few shapes, greatly simplifying the column design, electronics and data transfer requirements. The second major cost advantage is Multibeam's ability to build, test and optimize a single column, followed by a small column-array for further optimization and testing, before building a complete array of identical columns. This scalability reduces development time as well as cost.

Burn Lin of TSMC stated, "The goal for maskless is to have a machine that sells for $5 million euros and produces 10 wafers an hour."[12] Intel's Yan Borodovsky indicated last year, "Intel's 'rule of thumb' target for the economics of any next-generation lithography approach: US$0.5M in tool price for each wafer-per-hour (wph) throughput."[13] CEBL is able to meet this cost target.

In addition to meeting system capital cost requirements, CEBL eliminates a number of complex expensive masks, as well as simplifies processing, further reducing the cost of patterning each critical layer.

6. CONCLUSIONS

The 1D layout approach is extendable to the end of the ITRS roadmap. 1D lines have been demonstrated with optical lithography and pitch division to 16nm line/space[14] and 11nm line/space[15]. We expect this technique to be extended beyond 11nm line/space. With a resolution of 10 nm, Multibeam's technology is capable of cutting 11nm lines and beyond, as well as patterning via and contact layers.

The combination of 1D layouts, mature Optical lithography, and CEBL provides a viable solution that enables production of Logic and SoCs in HVM at future technology nodes.

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