Charting CEBL's Role in Mainstream Semiconductor Lithography

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ABSTRACT

E-Beam direct writing (EBDW) requires no masks and affords high resolution. But its slow writing speed has historically kept it out of mainstream fabs. Thanks to continuing EBDW advances combined with the industry's move to unidirectional (1D) gridded layout style, EBDW may soon provide a cost-efficient complement to 193nm ArF immersion (193i) optical lithography in high volume manufacturing (HVM).

Patterning conventional two-directional (2D) design layouts with 193i is a major roadblock in device scaling: the resolution limitations of optical lithography equipment have led to higher mask cost and increased lithography complexity. To overcome these challenges, IC designers have switched to 1D layouts with "lines and cuts" in critical layers.[1]

Leading logic and memory chipmakers have for several years been producing advanced designs with lines-and-cuts in HVM. However, cut masks in multiple optical patterning are getting extremely costly. Yan Borodovsky envisioned Complementary Lithography in which another lithography technology could be used to pattern line-cuts in critical layers to complement optical lithography.[2] Complementary E-Beam Lithography (CEBL) has emerged as a strong candidate to pattern the Cuts of optically printed Lines.

As the CEBL concept and other EBDW approaches continue to gain industry-wide awareness, concerns about throughput, scaling, and data preparation rate must be fully addressed. This paper examines the following issues:

- Challenges of massively parallel pixel writing (MPPW)
- Multiple mini-column design/architecture can:
    - Boost CEBL throughput
    - Resolve issues of CD control, CDU, LER, data prep rate, higher resolution, and 450mm wafers
- CEBL's role in next-generation semiconductor lithography

Keywords: CEBL, EBDW, Massively Parallel Pixel Writing, MPPW, Tennant's Law, 1D layout, Line and Cuts, 450mm

1. INTRODUCTION

Conventional EBDW, also called Maskless Lithography or ML2, writes one pixel at a time and has historically been too slow for use in production. In recent years, ML2 has evolved into massively parallel pixel writing (MPPW) to increase throughput, with hundreds of thousands of beamlets writing pixels in parallel.[3,4] The MPPW approach can improve throughput compared to conventional ML2, but scaling to higher resolution and 450mm wafers remains challenging. These issues will be examined.

Multibeam's CEBL approach deploys multiple miniature columns combined with vector scanning of shaped beams to boost throughput. The writing module is an array of mini-columns that cover the entire wafer area. Vector scan takes full advantage of the low density of CEBL line-cut patterns to reduce e-beam write time. Throughput can be further boosted by "clustering" multiple writing modules. These issues will be examined, along with Multibeam's solution to the data rate bottleneck. Also examined will be critical lithography issues such as CD control, CDU, LER and 450mm wafers.

As the industry continues to search for ways to mitigate the high cost of optical multiple patterning, the next-generation solution may emerge not as a single disruptive lithography technology, but rather some form of complementary lithographic techniques that work hands-in-hand with well-established optical methods.

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2. MASSIVELY PARALLEL PIXEL WRITING (MPPW)

2.1 Tennant's Law: Direct pixel writing challenges

Conventional EBDW, also known as Maskless Lithography or ML2, writes one pixel at a time and the writing speed is very slow. The limitation of conventional direct-write lithography was a topic of numerous studies for many years. D. M. Tennant, using available data circa 1995, plotted the relationship over a wide range between areal throughput (pixel writing speed) and resolution (feature size). The empirical observation, published in 1999 and now known as Tennant's Law, follows a power-law relationship.[5] The graph from Tennant's paper is reproduced in Figure 1.

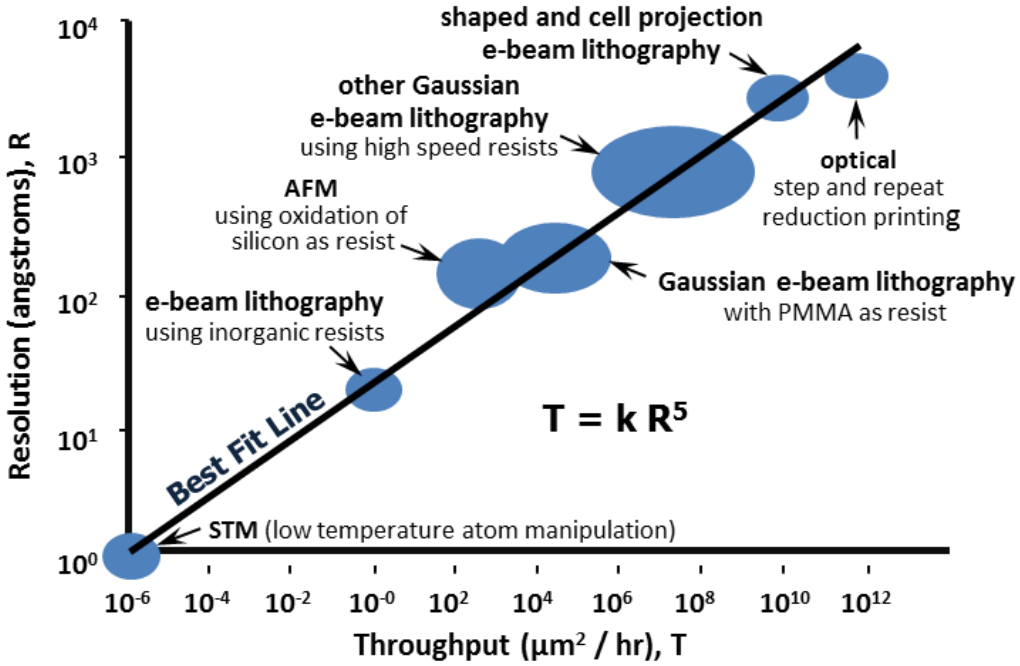

Figure 1. Tennant's Law: 30 years of empirical data mostly on e-beam pixel writing.

Tennant's Law is mainly about e-beam direct writing of pixels. The relationship between areal throughput T and resolution R can be represented by $T = k R^5$, where k is the proportionality constant and reflects the technology capability of the time. The value of k increased over the years as technology advanced but was unable to overcome the force of the power law.

Tennant's Law shows that throughput for direct-write lithography deteriorates rapidly with improving resolution. As shown in Table 1, when feature size (resolution) improves by 50%, throughput drops to 3%. The devastating effect of the 5th-power law underscores the enormous challenges facing ML2 pixel writing.

Table 1. ML2 pixel writing throughput drops drastically with improving resolution.

$T = k R^5$	
$R_{45} = 45nm$	T_{45}
$R_{22} = 22nm$	$T_{22} / T_{45} = (22/45)^5 = 0.028$

2.2 Key parameters to improve ML2 throughput

In ML2, operating parameters such as beam energy, beam current, and resist sensitivity can be optimized to improve e-beam write time. However, these parameters also tend to have opposing effects on resolution and throughput, as illustrated in Figure 2.[6] The utility of adjusting these parameters is limited, for example:

- Higher-energy e-beam can improve resolution, but it also lowers resist sensitivity and reduces throughput.
- Higher-current e-beam can boost writing speed, but it also broadens the beam, hurting resolution.
- More sensitive resist can shorten write time, but could result in pronounced shot noise and worse LER.
- Less sensitive resist can improve resolution, but slows writing speed
- High beam energy and/or current can cause local overheating of resist and wafer.

Figure 2. Key ML2 parameters work against each other.

2.3 Challenges of Massively Parallel Pixel Writing

Massively parallel pixel writing (MPPW) has evolved in recent years to overcome the throughput limitations of conventional ML2 observed in Tennant's Law.

In MPPW, a primary beam is split into many, from hundreds of thousands to one million, beamlets. These beamlets are raster-scanned over a wafer all at the same time, while the individual beamlets are turned on or off depending on whether there are pixels to write. MPPW could improve ML2 throughput with all beamlets writing pixels in parallel, but not without creating its own bottleneck.

As all one million beamlets in a column write simultaneously, pattern data must be sent to the column at an extraordinary high rate, on the order of 10 TB/s, at assumed throughput levels of $\leq$ 10 wph. This extreme data rate is currently unattainable and is a bottleneck in data preparation, or data bottleneck, in the MPPW approach.[7]

MPPW also faces other challenges when scaling to smaller features or 450mm wafer. Using Tennant's Law as a starting point (before any improvement is made), the total number of beamlets would have to increase by a factor of 2^5, or 32, to maintain the same throughput – each time the feature size is reduced by half. Similarly, as the industry transitions from 300mm to 450mm wafers, MPPW would have to increase total pixel writing speed 2.25 times to maintain throughput. This is shown in Table 2.

Table 2. MPPW scaling to smaller features and 450mm wafer while maintaining the same throughput

Number of Beamlets	Feature Size, nm	Wafer Size, mm
1 Million	45	300
32 Million	22	300
~1 Billion	11	300
~2.3 Billion	11	450

There are ways to improve MPPW pixel write time to maintain throughput as features scale, for example:

- Add more beamlets per column, or more columns per wafer, or both. MPPW columns are very complex. More beamlets per column add to column complexity; multiple columns for each wafer require stitching of patterned features at the pixel level. These solutions are challenging to implement and could increase system cost substantially.
- Redesign key components and subsystems, including the column, for each advancing node to optimize for pixel writing speed. This will drive up cost since each generation of an MPPW system is essentially good for only one node.
- Push operating parameters to enhance pixel writing speed or reduce pixel size, including faster wafer stage, higher or lower beam energy, beam current, and resist sensitivity. But these also have limitations.

These measures all aim to boost the value of k in Tennant's Law. Taking into account all the mitigation efforts, MPPW pixel writing speed could improve to the point where the 5^{th}-power law effectively becomes 4^{th}-power.

Viewed another way, the throughput-resolution relationship of well optimized MPPW could be represented by $T = k' R^{5}$, where k' reflects the new technologies available circa 2013 and may be much larger than k in conventional ML2. If k' is as large as 2k, for example, MPPW could be approximated by $T = k R^{4}$.

Thus, in the example of Table 2, at 22nm feature size, the number of beamlets would now increase to 16 million, rather than 32 million. Likewise, at the next 11nm feature, the number of beamlets would be about 250 million, not 1 billion. These are indeed very large improvements in MPPW throughput in scaling.

With extraordinary effort, MPPW writing speed could improve even further. However, the challenges to maintain performance quality, system reliability, and acceptable cost-of-ownership are considerable.

3. HOW MULTIBEAM'S CEBL ACHIEVES HIGH THROUGHPUT

Multibeam's solution to achieving high CEBL throughput is unique in the industry.[8,6] The three key factors that drive higher throughput in Multibeam's CEBL are:

3.1 Miniature columns

The Multibeam CEBL column is non-magnetic. It is like a typical SEM column without the magnetic field – and without the physically large electromagnetic coils that must be present to generate the magnetic field in the column. So the columns are small, and multiple miniature columns can be assembled in an array, covering an entire wafer.

Each Multibeam CEBL column has an electron source, deflection/blanking components, and focusing lens. Each column has only one beam; the beam does not split. Multibeam's CEBL writes each cut feature with a single exposure of a shaped beam, not pixel by pixel. Multibeam's CEBL write time does not degrade at smaller features or larger wafers (more on this later).

3.2 Vector scanning

Multibeam's CEBL writing strategy centers on vector scanning of the beam. In stark contrast, MPPW inefficiently raster-scans all the beamlets, sweeping over the entire wafer regardless of whether there are pixels to write.

In Multibeam's CEBL vector scan, a shaped beam is deflected to each cut feature, one shot per cut. Cut patterns are very low in density, ~5% or less. Thus, Multibeam's CEBL allows the beam to skip some 95% of the wafer area with no cut features, dramatically reducing write time.

Furthermore, Multibeam's multi-column design enables very high current density, about 10 times higher than today's e-beam mask writer. When vector scanning is combined with high current density and low pattern density, write speed is fast and throughput is high.

3.3 Scalable architecture

Multibeam's CEBL system is modular and scalable. Each multi-column array is a writing module, spanning the entire wafer. All beams in a module write independently and in parallel. A single module is capable of 5 wafers per hour, which is good for low volume production and chip development.

Multibeam's CEBL module is small in footprint, making it practical and cost-effective to integrate multiple modules within a single "cluster" system to achieve higher throughput and a higher level of redundancy. A 10-module cluster system, for example, is capable of 50 wafers per hour. Fig. 3 shows the scalability of Multibeam's approach to higher throughput.

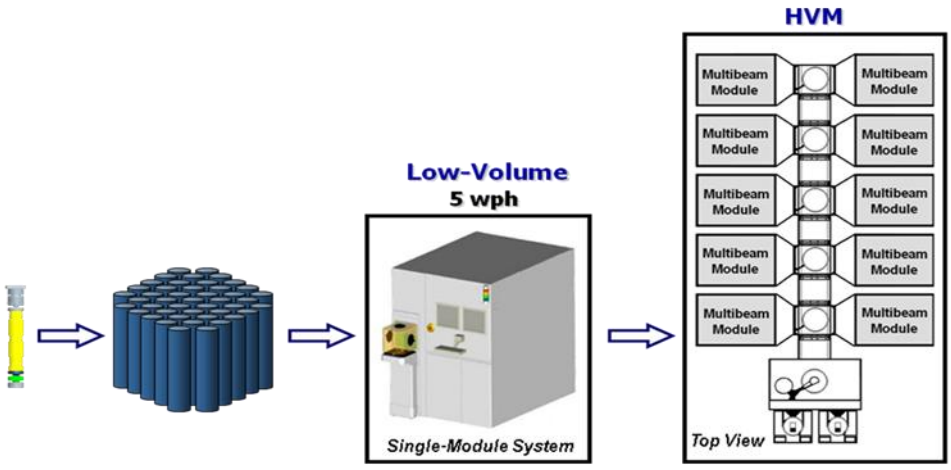

Figure 3. Multiple modules can be integrated in a cluster configuration for HVM.

4. HOW MULTIBEAM'S CEBL ADDRESSES CRUCIAL ISSUES

Among the crucial issues that may impact Multibeam CEBL's approach to semiconductor lithography are: control of line CD, CD uniformity (CDU), line-edge roughness (LER), data rate, and 450mm wafers.

4.1 CD, CDU, LER

In fabricating 1D "Lines-and-Cuts" layouts, the Lines define the CD in FEOL and BEOL patterns.

The CD is the conductor line width and is important as it may be a transistor gate length (for Lines in the Gate layer) or the metal line width (for Lines in the BEOL). The Lines are patterned with 193nm ArF immersion lithography which is proven capable of printing lines within tight tolerances in line-width control, CDU, and LER.

CEBL patterning the Cuts in the Lines does not change the already-defined line CD, CDU, and LER. In fact, CEBL Cuts have a much larger process window than Lines, since Cuts only have to separate line segments while providing sufficient overlaps for vias and transistor gates. This is illustrated in Fig. 4.

The self-aligned pitch division process, also known as self-aligned spacer process, is an accepted technique to reduce the pitch and increase line density. It is also capable of further improving LER of the Lines.

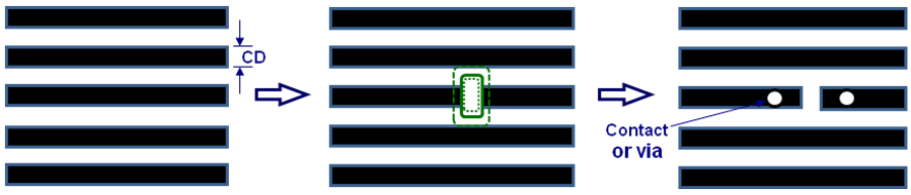

Figure 4. CEBL patterning of cuts and holes benefits from low pattern density and relaxed constraints.

4.2 Data bottleneck

Unlike Multibeam's one-beam-per-column approach, a MPPW column deploys a huge number of beamlets all of which are raster-scanned simultaneously. The pattern data is transferred to the MPPW column for turning each beamlet on or off in writing pixels. The data rate, on the order of 10 TB/s, is a severe bottleneck, as noted earlier.

Multibeam's CEBL writing module encompasses multiple mini-columns, about 100 columns for a 300mm wafer. Each independently controlled column receives and stores the pattern data, corrects errors, and directs the beam to the Cut features for patterning. All 100 columns in a module write independently and simultaneously.

Cut pattern density is sparse and Cut data volume is small. This small Cut database is partitioned and mapped to the 100 columns in the writing module. The partitioned data is then uploaded to all the column controllers in parallel. Parallel processing of Cut data is manageable with today's technology, circumventing the MPPW data bottleneck (See Fig. 6).

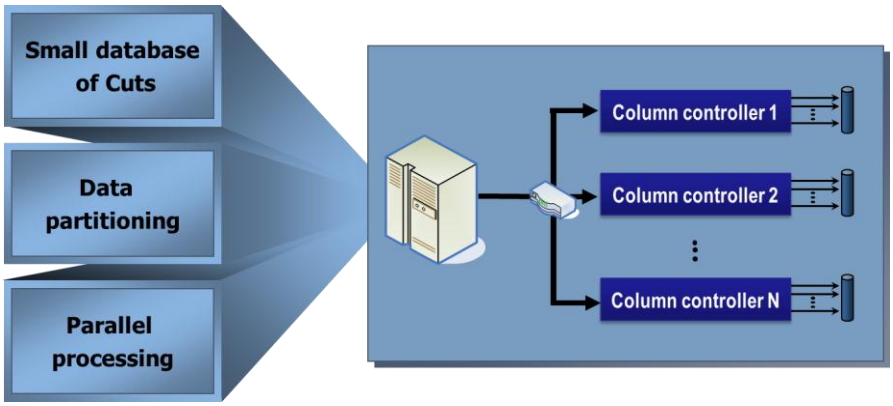

Figure 6. Multi-column CEBL circumvents the data prep bottleneck in MPPW

4.3 450mm wafer

Leading fabs are working on the transition to 450mm wafers. For MPPW, 450mm throughput drops to 44% of 300mm throughput, unless the already-large number of beamlets increases by 2.25 times, as previously noted.

In Multibeam's CEBL approach, the writing module is a column array that covers the whole wafer. Each column writes a 30x30mm area. Although columns may be added to the writing module for larger wafers, the writing area for each column remains the same. Thus, throughput is effectively independent of wafer size, as shown in Table 3.

Table 3. Multi-column CEBL scales to larger wafers without loss in throughput.

Wafer size	Number of columns per module	Throughput (10-module system)
200 mm	~50	50 wph
300 mm	~100	50 wph
450 mm	~200	50 wph

5. CONCLUSION

5.1 Multibeam's CEBL approach to achieve high throughput

Multibeam's approach to attaining high throughput and avoiding data bottlenecks may be summarized as follows:

- Vector scanning exploits the low pattern density of CEBL Cuts to the fullest
- Shaped-beam writing (one shot per Cut) avoids raster-scan pixel writing and skirts Tennant's Law
- Multiple columns writing independently and in parallel boost throughput dramatically
- Parallel processing of CEBL Cut data eliminates the daunting data bottleneck
- High current density, low pattern density, and vector scan combine to drastically reduce write time
- Scalable architecture enables high throughput for mainstream lithography

5.2 The next-generation solution of semiconductor lithography

Internet-capable mobile devices are now driving the IC market, demanding smaller size, less power, higher performance, and lower cost. As leading chipmakers march to serve this growth market, they must find ways to overcome the limitations of 193nm ArF lithography equipment while bringing down lithography cost.

As the lithography debate goes on, important developments have taken hold in the industry: 1D design layout is in high-volume production at mainstream fabs, Complementary Lithography is widely acknowledged as a potential cost-efficient solution, and CEBL development is well underway. Meanwhile, 193nm optical lithography and the indispensable photomasks keep the industry humming and growing.

Industry leaders are now coming to realize that the next-generation solution in lithography may not be a single technology à la optical dominance since the dawn of the industry a half-century ago. Rather, the next-gen solution is likely to be multiple lithographic technologies working in harmony with well-established optical lithography technologies to solve the unprecedented economic problem looming in semiconductor manufacturing.

In conclusion, three key technologies underpin a compelling Complementary solution:

- 193nm optical lithography together with photomasks will continue to pattern the uniform lines in 1D layouts. The Optical ecosystem with its mature technologies, innovative solutions, and advanced products will remain the bedrock of semiconductor lithography. Optical line-printing will be complemented by self-aligned pitch division to reduce pitch and increase line density if needed.[9,10]
- CEBL patterning will replace Optical Multiple Patterning of line-cuts and holes to reduce cost.[1,11,12] CEBL, too, will be complemented by other technologies in "hole shrinking" when CEBL cut size becomes so small that e-beam shot noise becomes unacceptable.
- 1D design layout is the technology that makes CEBL a compelling solution for reducing lithography cost. But there is still much to be gained from design-litho co-optimization. Designers and lithographers can work together to maximize the benefits of this new lithography paradigm.

Multibeam's ongoing CEBL development efforts promise to pave the way for EBDW to play a crucial role in reducing the cost of next-generation semiconductor lithography.

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