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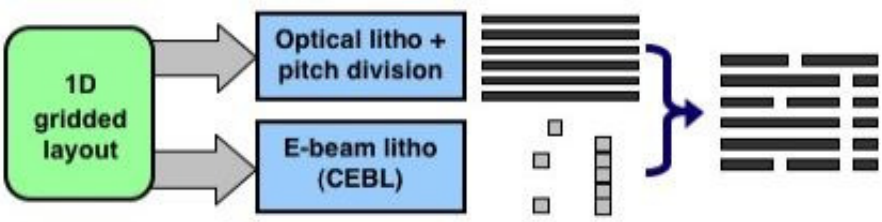
SPIE: A glimpse into Intel's litho future

by David K. Lam, Multibeam

March 7, 2011 - If anything in the litho world is certain, it's that 193nm ArF immersion lithography (193i) is being extended. Nikon's Masato Hamatani opened the Nikon LithoVision conference at this year's SPIE Advanced Lithography symposium, describing concrete efforts in improving overlay to less than 2nm and throughput to 4000 wafers per day. While EUVL is delayed by challenges in light sources, resist, and inspection tools, Nikon is ready with 193i to support multiple patterning at 20nm half-pitch.

At the 1x node, Hamatani described a "complementary lithography" approach, a concept first introduced at last year's LithoVision by Yan Borodovsky of Intel. "193nm immersion could work hand-in-hand with EUV or maskless lithography to enable advanced chip designs," stated Borodovsky then, showing a 20nm line/space pattern with 1D gridded layout that will benefit from EUV or EBDW for "line cuts" by avoiding quadruple patterning. In his SPIE 2011 talk, Hamatani assured the industry that it will be able to use a line-cutting approach -- and concluded with an intriguing remark that, besides efforts in 193i and EUV, Nikon is "considering other potential game-changers."

The twin themes of 193i extendability and complementary lithography appeared throughout LithoVision. TEL's Hidetami Yaegashi focused on 193i extendability, showing fascinating results in 193i pitch quadrupling, with line/space patterns at 25nm full pitch and hole patterns at 56nm pitch. In his estimation, at 22nm half-pitch, 193i with pitch division is lower-cost than EUV -- even if EUV reaches a throughput of 150 wafers per hour.



We saw a glimpse of Intel's vision for the future in Dr. Sam Sivakumar's presentation. He showed how Intel moved to 1-D design layouts at their 45nm node. The 1-D layout style (also known as unidirectional gridded layout) allowed Intel to use mature optical lithography tools, increasing process window and enabling a quick ramp. Because of the many benefits, Sivakumar stated that "Gridded layouts have now become ubiquitous -- the way of the future."

Looking ahead to the 14nm and 10nm nodes, Sivakumar noted EUV is late. This brought Sivakumar to the theme of his talk: Intel's design rules must remain compatible with optical multiple patterning and complementary lithography. Intel's design teams must be flexible and able to react quickly to implement EUV or e-beam lithography, enabling the company to take advantage of the most cost-effective lithography solution available.

David K. Lam and founded Lam Research in 1980; currently he heads up the David Lam Group, an investment and advisory firm for high-tech companies, and also chairman of Multibeam Corp. Contact: davidlam.com.
