E-beam Direct Write (EBDW) as Complementary Lithography

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ABSTRACT

193nm Optical lithography has powered the industry's growth for the last 10 years and multiple patterning is poised to extend 193nm even further. There is a growing trend in Logic design for manufacturing, with high-volume manufacturing (HVM) firms adopting a layout style using unidirectional single-pitch straight lines in poly and metal layers. These layouts lend themselves to a complementary lithography approach. First, unidirectional lines are patterned with Optical lithography. Second, these lines are "cut" to form the desired layout. In this paper, we present EBDW as a complement to optical lithography for line-cutting. We show how e-beam multiple-column architecture, optimized for line-cutting, is the best for patterning critical layers at advanced nodes as Complementary Lithography.

Keywords: E-Beam Lithography, EBDW, Complementary Lithography, 193nm resolution, Maskless Lithography, ML2, NGL, 1-D design layout

1. INTRODUCTION

Many in our industry think EBDW can't be used for high-volume manufacturing (HVM). There is some truth behind the skepticism, because EBDW is not economical to pattern every layer. However, EBDW can be highly cost-effective to *complement* Optical Lithography at advanced nodes – even in HVM.

2. EBDW IS PART OF THE INDUSTRY'S LITHO SOLUTION

Let's first take stock of the current lithography technology: 193nm ArF Lithography and 193nm Immersion. We'll call these 193 and 193i for short. This technology has powered the industry's growth for some 10 years. The technology is mature, so is the infrastructure. These reliable systems are produced by reputable companies and supported by capable engineers. 193/193i will continue to be the staple of high-volume chip production for years to come.

It is also well known that 193/193i is reaching its resolution limit. This is seen in the double patterning now used to pattern a single wafer layer. Optical challenges will only increase as geometries shrink. EBDW can help get around the Optical resolution problem. But EBDW is *not* the NGL (Next-Generation Lithography). EBDW will *not* replace Optical in HVM any time soon.

The semiconductor industry has been hard at work searching for a solution to the resolution challenge. Possible candidates include EUV, nano-imprint and EBDW. Of the three, the most viable and cost-effective solution is

EBDW if it is used to pattern critical layers, in a mix-and-match mode with 193i. Indeed, EBDW is crucial to our industry's future litho needs.

By focusing on low-density critical layers rather than patterning every layer, EBDW sidesteps its well-known weakness in low speed and exploits its unique advantage in high resolution. To HVM customers, this makes economic sense. For EBDW developers, this is the only path to HVM.

3. THE EVOLVING LOGIC DESIGN STYLE AND THE ROLE OF EBDW

In the role of complementary lithography, EBDW patterns only low pattern density critical layers, i.e. line-cuts, vias and contacts. While problematic vias and contacts have been well known to lithographers for years, the need to "cut lines" only emerged more recently among leading Logic manufacturers. But what are these "lines" and why is EBDW needed to "cut" them?

Optical resolution problems manifest themselves not just in mask costs but also in Logic device manufacturability. In recent years, the effort in DFM (Design for Manufacturing) has led to a new Logic design style in which the Poly and Metal layers are laid out in one direction and at a fixed pitch. Metal lines in one layer run perpendicular to those in the next level and are connected through vias. Sometimes referred to as 1-D GDR (One-Dimensional Gridded Design Rule), this design style is a drastic departure from the traditional 2-dimensional layout for Logics. To overcome the challenges in device manufacturability, conventional 2-D random Logic layouts is giving way to the new design style:

- Lars Liebmann has been promoting for years the idea of restrictive Logic design for manufacturability. IBM appeared to be adopting this highly regular, grating-like layout style for logic circuits in 2009[1].

- A TSMC press release[2] announced in June 2010 the completion of the "Slim Library" (at 65nm) using 1-D GDR layout for the poly layer, in collaboration with Tela Innovations. TSMC also stated that the logic areas were reduced by 15% with this new "lithography-optimized" layout pattern[2].

- An article on DFM was published in Intel Technology Journal[3] in 2008 showing a linear design style, with one pitch and one direction, implemented in the poly layer for a 45nm logic device.

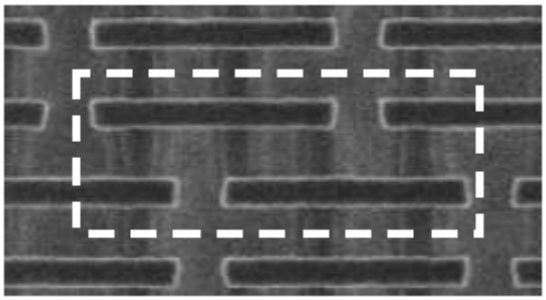

Figure 1: Intel 45nm node Logic poly layout[3]: one pitch and one direction

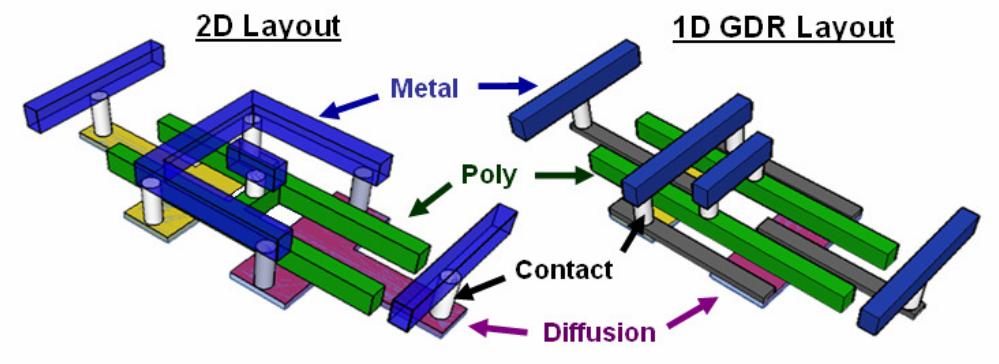

Figure 2: Conversion of CMOS layout from traditional 2-D design to 1-D GDR layout. Courtesy Tela Innovations

While leading Logic manufacturers are adopting the new design style – with unidirectional single-pitch lines – the continuity of these lines still has to be broken in fabricating the IC. In other words, lithography is needed to "cut" the lines. Following are three approaches being discussed by industry experts:

- Soichi Owa[4] of Nikon shows a roadmap to 11nm half-pitch with 193i used for both line-creation and line-cutting. To cut the lines, the all-optical approach will require double patterning at 22nm hp, quadruple patterning at 16nm hp (4 exposures and 4 etches, with 4 "cut" masks), and octuple patterning at 11nm hp (8 exposures and 8 etches, with 8 "cut" masks). While all-optical line-cutting calls to mind issues of process complexity, cycle time, and yield, in addition to cost of lithography and masks, it nevertheless represent one solution, as shown by Owa.

Half Pitch	L/S Formation for NAND and Logic	Logic (SRAM Gate) Cutting
22 nm	Spacer Doubling	Positive resist 2 Exposure, 2 etch
		Negative resist 2 Exposure, 2 etch
16 nm	Spacer Quadrupling	Positive resist 4 Exposure, 4 etch
		Negative resist 4 Exposure, 2 etch
11 nm ~10 nm	Spacer Quadrupling	Positive resist 8 Exposure, 8 etch
		Negative resist 4 Exposure, 2 etch

Figure 3: Nikon eReview, Spring 2010.[4] Excerpted from the original (Highlighted emphasis added by authors)

- Burn Lin of TSMC foresaw the complexity and cost of extending mask-based optical lithography[5,6,7,8,9]. He urges the industry to take EBDW seriously and put more resources behind EBDW development, to alleviate the mask-related problems facing the industry. He envisions foundries will ultimately use EBDW and believes EBDW "can be competitive in CoO, footprint, and environmental friendliness"[6].

- Yan Borodovsky of Intel presented the most realistic solution at the LithoVision Symposium[10] during the week of SPIE Advanced Lithography Conference in February 2010 and again at the Maskless Litho

Workshop[11] in May 2010. He, too, recognizes that an all-optical approach can do the job of cutting lines at 20nm hp, with quadruple patterning. But he also points out that EBDW can cut lines and eliminate all four "cut" masks. Used this way, EBDW complements Optical. As "Complementary Lithography" – a term first coined by Borodovsky – EBDW patterns critical layers in a mix-and-match mode with Optical 193/193i.

The use of EBDW to complement Optical will indeed take advantage of the best of both lithography technologies.

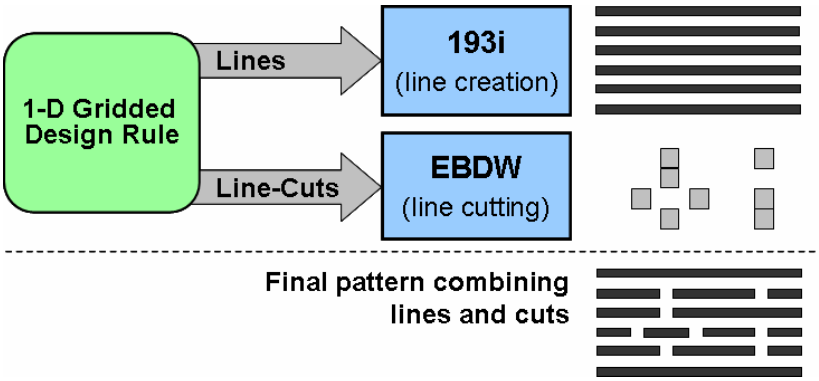

Figure 4: This is Complementary Lithography. A layout with 40nm pitch requires Optical litho with four "cut" masks, or EBDW with zero "cut" masks.

4. THE STRATEGY TO IMPLEMENT COMPLEMENTARY LITHOGRAPHY

Following are four strategic steps to implement EBDW as Complementary Lithography.

Pattern critical layers only	**Low-density patterns: ~5%**
Vector-scan shaped beam	**Lower overhead, reduce data storage and reduce data transfer to each column**
Array multiple columns	**Scalable architecture to boost throughput**
Cluster multiple modules	**Clustering to meet HVM requirements**

Figure 5: Implementation Strategy for EBDW as Complementary Lithography

1. Focus on patterning critical layers. Critical layers, i.e. line-cuts, via and contact holes, have low pattern density, typically at about 5%. Focusing on critical layers avoids much of EBDW's speed deficiency.

2. Vector-scan shaped beams. Vector scanning allows the beam to skip over empty areas with no patterns, saving overhead. When patterning with a vector scanned shaped beam, the data path is greatly simplified, requiring only a few parameters, such as x and y for location and t for dose, for each line-cut, via or contact. This drastically reduces data transfer rate to each column.

3. Array multiple columns. If the column diameter is small enough, multiple columns can be packed in an array to boost throughput. The multi-column array is the heart of an EBDW wafer-patterning module.

4. Cluster multiple modules. To meet the high throughput requirements of HVM, it is necessary to integrate multiple wafer-patterning modules into a cluster tool. Each EBDW module has a small cleanroom footprint, enabling the cluster tool to meet overall footprint and cost-of-ownership requirements.

5. AN EXAMPLE OF EBDW IMPLEMENTATION FOR HVM: MULTIBEAM CORP.

Multibeam Corp. is implementing EBDW specifically for critical layer patterning as Complementary Lithography. Here, we examine two aspects of its approach:

1. **An all-electrostatic column**
2. **Column array architecture**

Multibeam's column design leverages publicly available industry knowledge in e-beam lithography technology developed over 30 years. Industry know-how extends to the production environment, where e-beam is used today in mask making and wafer inspection. Multibeam uses commercial column design software, enhanced with proprietary software, to optimize and simulate the e-beam column to pattern line-cuts, vias and contacts.

A major innovation is the introduction of all-electrostatic lenses. Eliminating magnetic hysteresis enables high-speed beam deflection for shaping, blanking and positioning the beam on the wafer surface. Eliminating the magnetic coil allows the column to be very thin and amenable to a multi-column array architecture.

Multibeam's column design is optimized for Complementary Lithography:

- One beam per column
- Vector-scanned shaped beams
- Adjustable e-beam landing energy to improve LWR and CDU
- High resolution, extendable to future technology nodes

The column has another important and unique feature: every column has an electron detector. The signal from this detector is used to calibrate the beam shape and size to ensure the system meets LER and CDU requirements. Used in 'SEM mode', the detector images local alignment marks to improve Overlay accuracy.

Building these columns is an engineering challenge, but not a technological hurdle. By focusing on patterning critical layers mixed-and-matched with Optical, the scope of application engineering is significantly narrowed. By optimizing a single e-beam column before building a column-array of identical columns, development time and cost are greatly reduced.

Multibeam's e-beam column-array is expandable with identical columns to increase throughput. For high throughput, about 100 columns span the surface of a 300mm wafer. The column-array scales for any wafer size, including 450mm, with the same throughput.

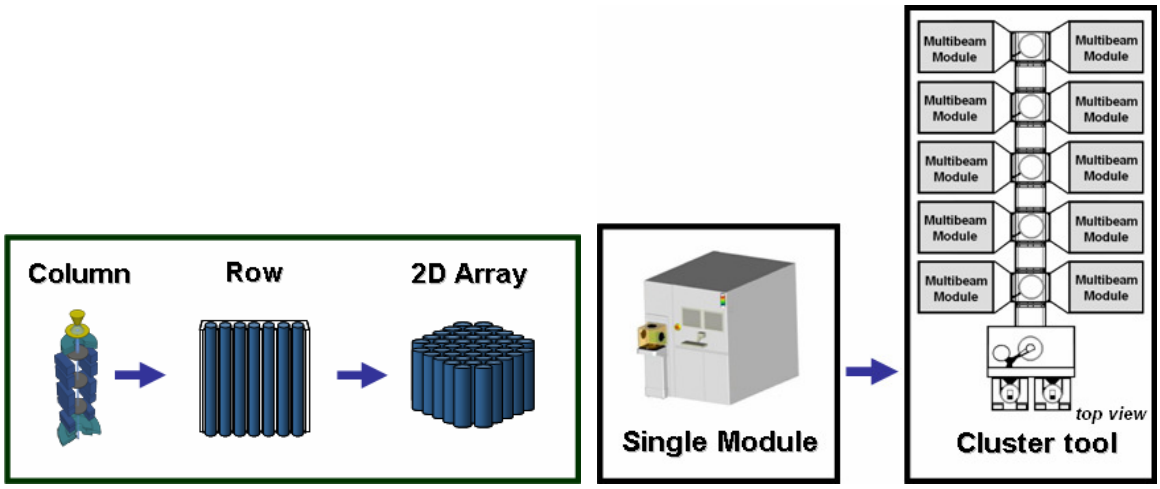

Figure 6: Multibeam scalable architecture. A 2D Array of identical columns optimized for Complementary Lithography.

6. THE NGL IS HERE

The NGL we are waiting for is not a single, monolithic lithography technology replacing Optical wholesale. The advantages of 193/193i technology are too important to ignore. The wisdom of not "throwing out the baby with the bath water" holds true in the debate of the future of 193/193i. EBDW requires no new support infrastructure, as it is compatible with existing infrastructure in the industry. With EBDW patterning critical layers to complement Optical, our customers will benefit from lower cost, simpler process, shorter cycle time and higher yield.

As a developer of EBDW, our goal is not to be the NGL, but to help alleviate the most troubling resolution problems plaguing the industry. 193/193i Optical Litho combined with Complementary EBDW is the "NGL".

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